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European Patent Office
Office européen des brevets



(11) Publication number:

0 557 968 A2

(12)

EUROPEAN PATENT APPLICATION

(21) Application number: 93102875.7

(51) Int. Cl.⁵: G11C 16/06, G11C 11/00

(22) Date of filing: 24.02.93

(30) Priority: 25.02.92 JP 73255/92

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(43) Date of publication of application:
01.09.93 Bulletin 93/35

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(84) Designated Contracting States:
DE FR GB

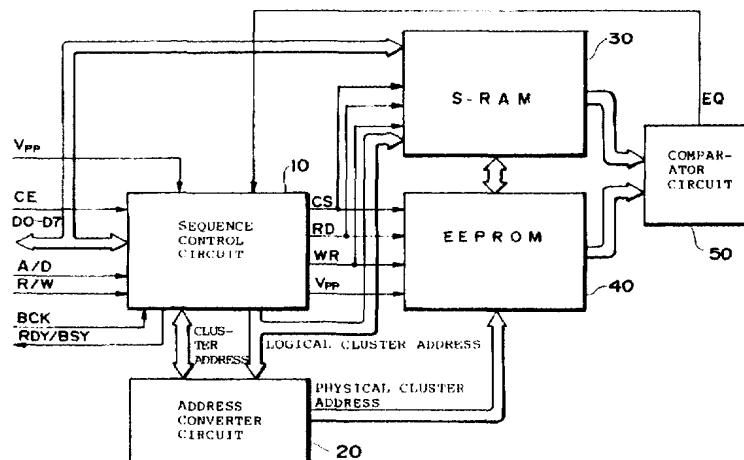
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(54) Method of rewriting data in EEPROM, and EEPROM card.

(57) A memory card includes an S-RAM in addition to an EEPROM. When old data constituting part of data that has been recorded in the EEPROM is to be rewritten, the old data to be rewritten is read out of the EEPROM and applied to the S-RAM, where the old data is temporarily stored. The old data in the S-RAM is rewritten to new data, and the new data is applied to and written in the EEPROM. A comparator

circuit determines whether all bits of the new data rewritten in the S-RAM and all bits of the new data written in the EEPROM coincide. If all bits coincide, this is verification that the changed data has been stored in the EEPROM correctly. Thus, the reliability with which data is rewritten in the EEPROM is improved.

Fig. 1



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BACKGROUND OF THE INVENTION**Field of the Invention:**

This invention relates to a method of rewriting data in an EEPROM (electrically erasable programmable read-only memory), as well as to an EEPROM card. Description of the Related Art:

Memory cards of the type incorporating an S-RAM (static random-access memory) inside a case are disadvantageous in that battery back-up is required and the unit price per bit is high. Accordingly, the development of memory cards equipped with an EEPROM designed to eliminate these drawbacks is proceeding. Though a memory card having an internal EEPROM is advantageous in that battery back-up is unnecessary while the unit price per bit is low, the number of rewriting operations possible is on the order 10,000. In terms of reliability, therefore, a memory card of this type is inferior to the card having the internal S-RAM.

SUMMARY OF THE INVENTION

An object of the present invention is to improve the reliability with which data can be rewritten in an EEPROM.

According to the present invention, the foregoing object is attained by providing a method of rewriting an EEPROM card comprising a step of addressing an area of an EEPROM in which first data that includes old data to be rewritten has been stored and reading out the first data that has been stored in this area, a step of writing the first data, which has been read out of the EEPROM, in a RAM, a step of generating second data in the RAM by rewriting new data for the old data in the first data that has been written in the RAM, a step of addressing an area of the EEPROM in which the second data, which includes the new data, is to be written, and writing the second data, which has been read out of the RAM, in this area, and a step of reading the second data out of the RAM, reading the second data, which has been written in the EEPROM, out of the EEPROM, and determining whether the second data read out of the RAM and the second data read out of the EEPROM coincide.

Further, according to the present invention, the foregoing object is attained by providing an EEPROM card comprising an EEPROM in which data is capable of being erased and written, a RAM for performing an operation through which data in the EEPROM is updated, first data reading/writing means for addressing an area of the EEPROM in which first data that includes old data to be rewritten has been stored, reading out the first data that has been stored in this area and writing the first data, which has been read out of the EEPROM, in

the RAM, data updating means for generating second data by rewriting new data for the old data in the first data that has been written in the RAM, data writing means for addressing an area of the EEPROM in which the second data, which has been rewritten by the data updating means, is to be written, and writing the second data in this area, and discriminating means for comparing the second data in the RAM, which data has been rewritten by the data updating means, and the second data that has been written in the EEPROM by the data writing means, and determining whether the rewritten second data in the RAM and the second data written in the EEPROM coincide.

In accordance with the invention, the first data containing the old data to be rewritten is read out of the EEPROM and written in the RAM. The old data in the first data that has been written in the RAM is rewritten into new data, whereby second data is produced. The second data is written in the EEPROM.

In an embodiment of the invention, an area of the EEPROM from which the first data is read out and an area of the EEPROM in which the second data is written are the same area.

In one embodiment of the invention, when it is determined that the second data in the RAM does not coincide with the second data in the EEPROM, the second data is written in another area of the EEPROM. It is again determined whether the second data in the RAM coincides with the second data that has been written in the other area of the EEPROM.

In another embodiment of the invention, when it is determined that the second data in the RAM does not coincide with the second data in the EEPROM, the writing of the second data in the EEPROM is performed again a prescribed plurality of times until it is determined that the second data in the RAM coincides with the second data in the EEPROM. When a determination of coincidence is not obtained even when the writing of the second data in the above-mentioned area of the EEPROM is performed again the prescribed plurality of times, the second data is written in the other area of the EEPROM.

In accordance with the present invention, a check is performed at all times to determine whether new data (the second data) following a change has been written in the EEPROM correctly, and therefore the reliability of the EEPROM is improved. When it is determined that writing has not been performed correctly, the writing of the second data in the same area or another area is performed again. As a result, the reliability with which data is rewritten in the EEPROM is improved. Since data in the first data other than the old data that is to be rewritten is preserved by being written in the RAM,

loss of data caused by a data writing failure or by a defect in the EEPROM is prevented.

Other features and advantages of the present invention will be apparent from the following description taken in conjunction with the accompanying drawings, in which like reference characters designate the same or similar parts throughout the figures thereof.

BRIEF DESCRIPTION OF THE DRAWINGS

- Fig. 1 is a block diagram illustrating the electrical configuration of a memory card;
- Fig. 2 is block diagram showing the configuration of a sequence control circuit;
- Fig. 3 is a block diagram showing the configuration of an address converter circuit;
- Figs. 4a and 4b are diagrams showing examples of a logical cluster area and examples of a physical cluster area, respectively;
- Figs. 5a, 6a, 7a, 8a and 9a are diagrams showing the manner in which data in the logical cluster area changes; and
- Figs. 5b, 6b, 7b, 8b and 9b are diagrams showing the manner in which data in the physical cluster area changes.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Fig. 1, which illustrates an embodiment of the present invention, is a block diagram showing the electrical circuit configuration incorporated within the case of a memory card.

A memory card includes a sequence control circuit 10, by which the overall operation of the card is supervised, an address converter circuit 20 for generating addresses, an S-RAM 30, and an EEPROM 40 for storing digital data. The S-RAM 30 is used in order to perform an operation through which data is updated. Data to be written in the EEPROM 40 is stored temporarily in the S-RAM 30.

In order to verify whether data has been written in the EEPROM 40 with certainty, data that has been stored temporarily in the S-RAM 30 is compared with data that has been written in the EEPROM 40. To this end, the memory card contains a comparator circuit 50. If the data that has been stored temporarily in the S-RAM 30 coincides with the data that has been written in the EEPROM 40, the comparator circuit 50 outputs a coincidence signal EQ, after which the data that has been stored in the S-RAM 30 is erased.

Applied to the sequence control circuit 10 from an electronic device (such as an electronic still-video camera), in which the memory card is removably loaded, are a program supply voltage VPP, a

card-enable signal CE, image data (data to be written or read) or address data (which designates the location for the writing or reading of the data) D0 ~ D7, a data identifying signal A/D that represents whether the data D0 ~ D7 is image data or address data, a write/read signal R/W that represents the writing of image data to the memory card or the reading of image data from the memory card, and a bus clock pulse BCK. These signals arrive from the electronic device through a connector. The data D0 ~ D7 is applied to the S-RAM 30 as well.

The sequence control circuit 10 outputs a status signal RDY/BSY, which represents whether the memory card is in a state (READY) in which it is capable of sending and receiving image data or address data or in a state (BUSY) in which it is incapable of sending and receiving image data or address data. The electronic device in which the memory card has been loaded is provided with the signal RDY/BSY via the connector.

Fig. 2 illustrates an example of the construction of the sequence control circuit 10.

As shown in Fig. 2, the sequence control circuit 10 includes a command control circuit 11 and an address register 12.

The above-mentioned data identifying signal A/D, write/read signal R/W and bus clock pulse BCK are fed into the command control circuit 11, which outputs a chip select signal CS, a memory read signal RD and a memory write signal WR. The chip select signal CS, memory read signal RD and memory write signal WR are outputted from the sequence control circuit 10 and applied to the EEPROM 40 and S-RAM 30. The command control circuit 11 outputs the status signal RDY/BSY.

The command control circuit 11 also outputs a latch clock pulse, which is applied to the address register 12. The latter is provided with the data D0 ~ D7. A logical cluster address that designates the address of a logical cluster area contained in the address converter circuit 20 is generated within the address register 12.

The sequence control circuit 10 and address converter circuit 20 send and receive cluster address data to and from each other. The cluster address data includes the address of a logical cluster that designates a cluster in which a data writing error has occurred, the address of a last-written cluster in which writing has been performed last, and the address of a write cluster (over-written cluster address) in which over-writing has been performed.

Fig. 3 illustrates an example of the construction of the address converter circuit 20.

As shown in Fig. 3, a memory contained in the address converter circuit 20 is provided with a logical cluster area 21. As shown in Fig. 4a, the

logical cluster area 21 stores, in correspondence with logical cluster addresses, the physical cluster addresses designated by these logical cluster addresses. When a logical cluster address is applied, the physical cluster address designated by this logical cluster address is read out of the logical cluster area 21 and delivered as an output. This physical cluster address is applied to the EEPROM 40.

When it is determined whether the data that has been stored in the S-RAM 30 coincides with the data that has been written in the EEPROM 40, those items of data are read out of the S-RAM 30 and EEPROM 40 and applied to the comparator circuit 50, as set forth above. The comparator circuit 50 compares these items of data and outputs the coincidence signal EQ when the two items of data coincide. The coincidence signal EQ is applied to the sequence control circuit 10.

Figs. 4a through 9b schematically represent the cluster areas. Figs. 4a, 5a, 6a, 7a, 8a and 9a represent the logical cluster area provided in the address converter circuit 20, and Figs. 4b, 5b, 6b, 7b, 8b and 9b represent the physical cluster area provided in the EEPROM 40.

The term "cluster" refers to a unit of data written to or read from the memory. The rewriting of data is carried out one cluster at a time. In terms of image data, compressed image data that represents one frame of an image is an amount of data equivalent to one cluster or several clusters. The term "physical cluster area" refers to an area in which data is actually stored in the EEPROM 40, and the term "physical cluster address" refers to an address of a location at which data is stored. The term "logical cluster area" refers to an area used in order to manage the physical cluster addresses.

As illustrated in Fig. 4a, the logical cluster area stores the physical cluster addresses in correspondence with logical cluster addresses ad1 ~ ad8 of this area. In Fig. 4a, physical cluster addresses have not yet been written (i.e., the data has been initialized to all "0"s). The address converter circuit 20 is further provided with an area for storing a last-written physical cluster address and an over-written logical cluster address. As shown in Fig. 4b, the physical cluster area stores one cluster of data, for every address, in correspondence with physical cluster addresses AD1 ~ AD12. In Fig. 4b, data has not yet been written and the area is in a "blank state" (all "0"s). Addresses up to ad8 are shown with regard to the logical cluster area and up to AD12 with regard to the physical cluster area. However, it goes without saying that these areas may be provided with more storage locations as the need arises.

When the READY signal is outputted by the sequence control circuit 10 and the writing of data in the EEPROM 40 is performed, the image data D0 ~ D7 is applied to the memory card. The image data D0 ~ D7 is applied to the S-RAM 30 and, via the S-RAM 30, to the EEPROM 40.

The write/read signal R/W representing the writing operation is applied to the sequence control circuit 10. On the basis of this signal, the sequence control circuit 10 outputs the memory write signal WR, which is applied to the S-RAM 30 and EEPROM 40. As a result, the image data is stored in the S-RAM 30.

Furthermore, the sequence control circuit 10 outputs logical cluster addresses, which are applied to the address converter circuit 20 and the S-RAM 30. As a result of applying the logical cluster addresses to the S-RAM 30, that image data, which has been stored in the S-RAM 30, designated by the logical cluster addresses is applied to the EEPROM 40.

The logical cluster addresses are applied to the address converter circuit 20 and, as shown in Fig. 5a, physical cluster addresses are stored in the logical cluster area. These physical cluster addresses are applied to the EEPROM 40. As a result, the image data provided by the S-RAM 30 is stored in the physical cluster area designated by the physical cluster addresses of the logical cluster area. This state is illustrated in Fig. 5b. Data A₁, B₁, C₁ and D₁ is contained in one item of cluster data CLD1 stored at physical cluster address AD1. Similarly, items of cluster data from CLD2 to CLD8 respectively containing data from A₂, B₂, C₂ and D₂ to A₈, B₈, C₈ and D₈ are stored at the other physical cluster addresses from AD2 to AD8. Though it is described that eight items of cluster data are stored in the EEPROM 40 at one time, it goes without saying that an arrangement may be adopted in which the data is written one cluster at a time or a plurality of clusters at a time. Further, in the same manner as in the case of the rewriting of data described here, image data that has been stored in the S-RAM 30 and the corresponding image data that has been written in the EEPROM 40 are compared one cluster at a time in the comparator circuit 50, and it is determined whether the writing of the data in the EEPROM 40 has been performed correctly.

In the case set forth above, the writing of digital data is performed when all of the storage locations of the physical cluster area are blank, and over-writing is not carried out. Therefore, data "0" is stored as the over-written logical cluster address and data "AD8" is stored as the last-written physical cluster address, as shown in Fig. 5a.

Assume that rewriting of the data that has been stored at the physical cluster address AD2 is per-

formed. In such case, the cluster data CLD2 (A_2 , B_2 , C_2 , and D_2) that has been stored at the physical cluster address "AD2" is read out and applied to the S-RAM 30, where the data is stored. Partial rewriting of the data (rewriting of old data D_2 to new data E_2) is performed in the S-RAM 30. More specifically, the data $D_0 \sim D_7$ representing the data E_2 is applied to the S-RAM 30, and this data is substituted for the old data D_2 .

The cluster data CLD2 partially rewritten in the S-RAM 30 is applied to the EEPROM 40. The address converter circuit 20 outputs "AD2" as the data of the physical cluster address, and this data is applied to the EEPROM 40. As a result, new cluster data CLD2 (A_2 , C_2 , D_2 , and E_2) is stored at the storage location of the physical cluster address "AD2" in the physical cluster area. The new cluster data may thus be stored at the original storage location or at a different storage location in the physical cluster area.

The item of data (the cluster data CLD2 after rewriting) temporarily stored in the S-RAM 30 and the item of data (the new cluster data CLD2) written in the EEPROM 40 are each read out and applied to the comparator circuit 50. The comparator circuit 50 compares these two clusters and outputs the coincidence signal EQ if all bits coincide. This signal is applied to the sequence control circuit 10. As a result, the sequence control circuit 10 verifies that the rewriting of the cluster data CLD2 in the EEPROM 40 has been performed correctly.

If coincidence is not achieved, it is construed that the storage location of the physical cluster address "AD2" is a defective area and this location is no longer used for storage of cluster data. The new cluster data CLD2 (A_2 , C_2 , D_2 , and E_2) that has been rewritten in the S-RAM 30 is written at the storage location of the "blank" physical cluster address "AD9" instead of the storage location of the physical cluster address "AD2". This state is illustrated in Figs. 6a and 6b. At this time the last-written physical cluster address is incremented and "AD9" is stored.

In the description given above, the cluster data CLD2 that has been rewritten in the S-RAM 30 is written in the EEPROM 40, after which the items of cluster data are read out of the S-RAM 30 and EEPROM 40 and compared. If these items of data do not coincide, a judgment is made that the storage location of address AD2 in the EEPROM 40 is faulty. It is preferred to adopt an arrangement in which the writing of the cluster data at the storage location of address AD2 in the EEPROM 40 and the comparison of the cluster data of the S-RAM 30 with the corresponding cluster data that has been written in the EEPROM 40 be carried out repeatedly a plurality of times until a result indicative of coincidence is obtained, without judging that

a storage location is faulty based upon only a single comparison. When a result indicative of coincidence is not obtained even if this processing is repeated a plurality of times, the storage location at address AD2 is judged to be defective.

Operation will now be described for a case in which the cluster data CLD4 at the storage location of address AD4 is shifted to the storage location of address AD3 in the physical cluster area. First, it is necessary to shift the cluster data CLD3 at address AD3 to another location, e.g., the storage location of address AD10.

As shown in Fig. 7a, the address AD10 of the physical cluster area is written to correspond to the logical cluster address ad3 in the logical cluster area. In order to store the fact that the data at this address ad3 has been over-written, "ad3" is written in as the over-write logical cluster address.

The cluster data CLD3 at address AD3 in the physical cluster area is read out and stored temporarily in the S-RAM 30. Thereafter, the cluster data CLD3 is transferred from the S-RAM 30 to the storage location designated by the address AD10 of the EEPROM 40. This is the state illustrated in Fig. 7b. The last-written physical cluster address is updated to AD10.

In this case also, the cluster data CLD3 that has been stored in the S-RAM 30 and the cluster data CLD3 that has been stored at address AD10 of the EEPROM 40 are compared to determine whether the writing of the cluster data in the EEPROM 40 has been performed correctly.

Next, in order to shift the cluster data CLD4 at the physical cluster address AD4 to address AD3, the data at the logical cluster address ad4 is updated to AD3 and the data of over-written logical cluster address AD4 is updated to ad4 (see Fig. 8a). Once the cluster data at the physical cluster address AD4 has been transferred to and stored in the S-RAM 30, this cluster data is written in the storage location at address AD3 of the physical cluster area (see Fig. 8b). The storage location at address AD4 becomes blank. The last-written physical cluster address remains unchanged at "AD10".

In a case where part of the cluster data CLD5 designated by the physical cluster address "AD5" is changed in Figs. 8a and 8b, the cluster data CLD5 (A_5 , B_5 , C_5 and D_5) at this address is read out and transferred to the S-RAM 30, where a partial change of the data (a change from data D_5 to data E_5) is performed.

The changed new cluster data CLD5 (A_5 , B_5 , C_5 and E_5) is applied to the EEPROM 40 and written in the blank storage location at address "AD4". The new cluster data CLD5 that has been written in the storage location at address "AD4" is read out of the EEPROM 40 and applied to the

comparator circuit 50. The cluster data CLD5 after the change, which data has been stored in the S-RAM 30, is also applied to the comparator circuit 50.

The comparator circuit 50 performs a comparison to determine whether the cluster data CLD5 after the change read out of the S-RAM 30 and the new cluster data CLD5 read out of the EEPROM 40 coincide. If the comparison indicates non-coincidence, it is judged that the writing of the new data in the EEPROM 40 has failed. As a result, the new data is written in the blank storage area at address "AD11". In this case also, the new items of cluster data are read out of the EEPROM 40 and S-RAM 30 and the comparator circuit 50 determines whether these items of data coincide.

The state in which new data has thus been written at the physical cluster address "11" is illustrated in Figs. 9a and 9b. In this case, the overwritten logical cluster address is changed to "ad5" and the last-written physical cluster address is changed to "AD11", as illustrated in Fig. 9a.

As many apparently widely different embodiments of the present invention can be made without departing from the spirit and scope thereof, it is to be understood that the invention is not limited to the specific embodiments thereof except as defined in the appended claims.

Claims

1. A method of rewriting data in an EEPROM comprising the steps of:
 - addressing an area of an EEPROM in which first data that includes old data to be rewritten has been stored and reading out said first data that has been stored in this area;
 - writing said first data, which has been read out of the EEPROM, in a RAM;
 - generating second data in the RAM by rewriting new data for said old data in said first data that has been written in the RAM;
 - addressing an area of the EEPROM in which said second data, which includes said new data, is to be written, and writing said second data, which has been read out of the RAM, in this area; and
 - reading said second data out of the RAM, reading said second data, which has been written in the EEPROM, out of the EEPROM, and determining whether said second data read out of the RAM and said second data read out of the EEPROM coincide.
2. The method according to claim 1, wherein an area of the EEPROM from which said first data is read out and an area of the EEPROM in which said second data is written are the same

area.

3. The method according to claim 1, further comprising a step of writing said second data in another area of the EEPROM when it is determined that said second data in the RAM does not coincide with said second data in the EEPROM.
4. The method according to claim 3, further comprising a step of determining again whether said second data in the RAM coincides with said second data that has been written in the other area of the EEPROM.
5. The method according to claim 1, wherein when it is determined that said second data in the RAM does not coincide with said second data in the EEPROM, the writing of the second data in the EEPROM is performed again a prescribed plurality of times until it is determined that said second data in the RAM coincides with said second data in the EEPROM.
6. The method according to claim 5, wherein when a determination of coincidence is not obtained even when the writing of said second data in the area of the EEPROM is performed again said prescribed plurality of times, said second data is written in another area of the EEPROM.
7. An EEPROM card comprising;
 - an EEPROM in which data is capable of being erased and written;
 - a RAM for performing an operation through which data in said EEPROM is updated;
 - first data reading/writing means for addressing an area of said EEPROM in which first data that includes old data to be rewritten has been stored, reading out the first data that has been stored in this area and writing the first data, which has been read out of said EEPROM, in said RAM;
 - data updating means for generating second data by rewriting new data for the old data in the first data that has been written in said RAM;
 - data writing means for addressing an area of said EEPROM in which the second data, which has been rewritten by said data updating means, is to be written, and writing the second data in this area; and
 - discriminating means for comparing the second data in said RAM, which data has been rewritten by said data updating means, with the second data that has been written in said EEPROM by said data writing means, and

determining whether the rewritten second data in the RAM and the second data written in said EEPROM coincide.

8. The EEPROM card according to claim 7, further comprising control means for controlling said data writing means in such a manner that said second data is written in another area of said EEPROM when it is determined that the second data in said RAM does not coincide with the second data in said EEPROM. 5

9. The EEPROM card according to claim 7, further comprising control means for controlling said data writing means in such a manner that when it is determined that the second data in said RAM generated by said data updating means does not coincide with the second data written in said EEPROM by said data writing means, the writing of the second data in said EEPROM is performed again a prescribed plurality of times until it is determined that the generated second data in the RAM coincides with the second data in said EEPROM. 10 15 20

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40

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50

55

Fig. 1

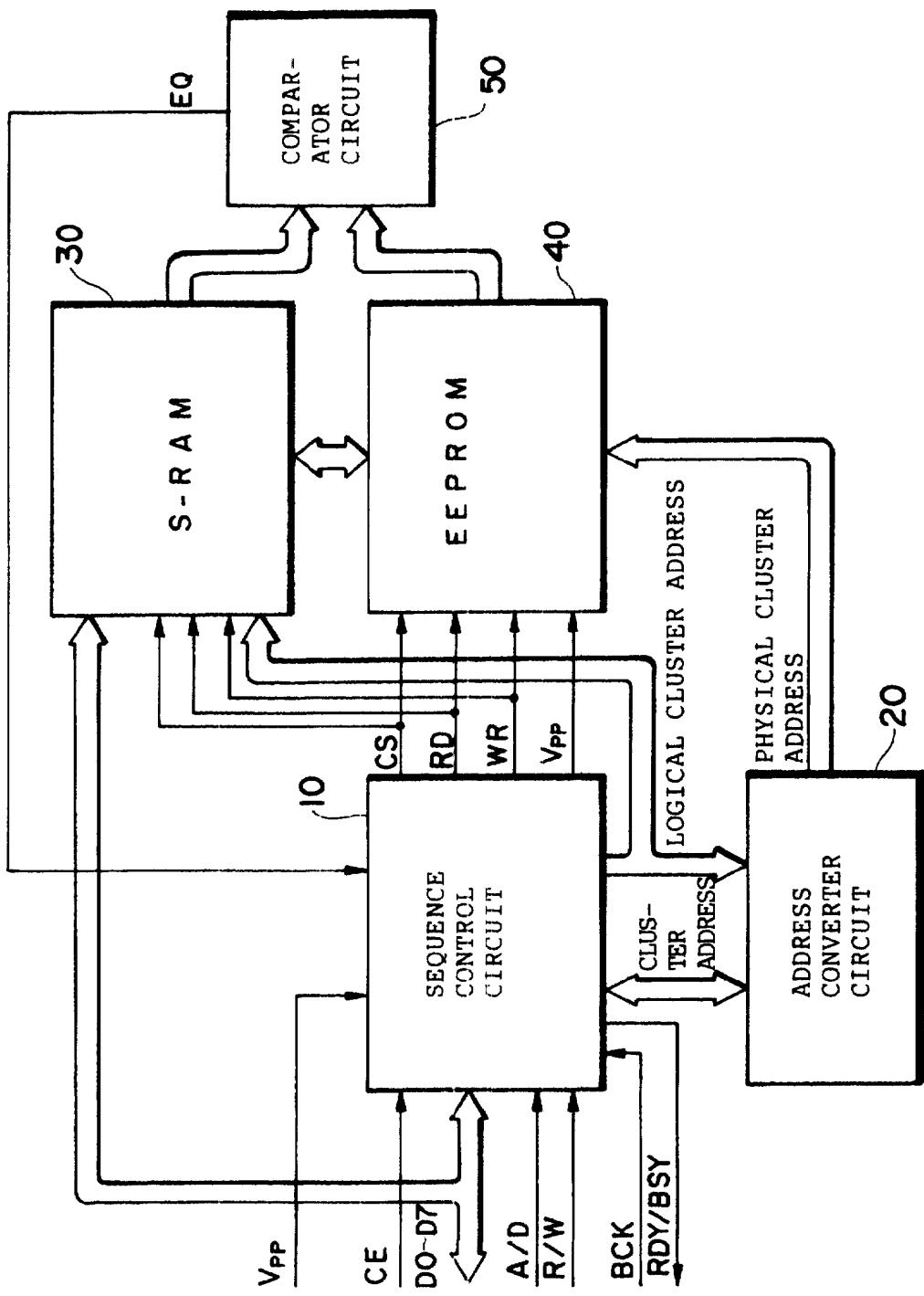


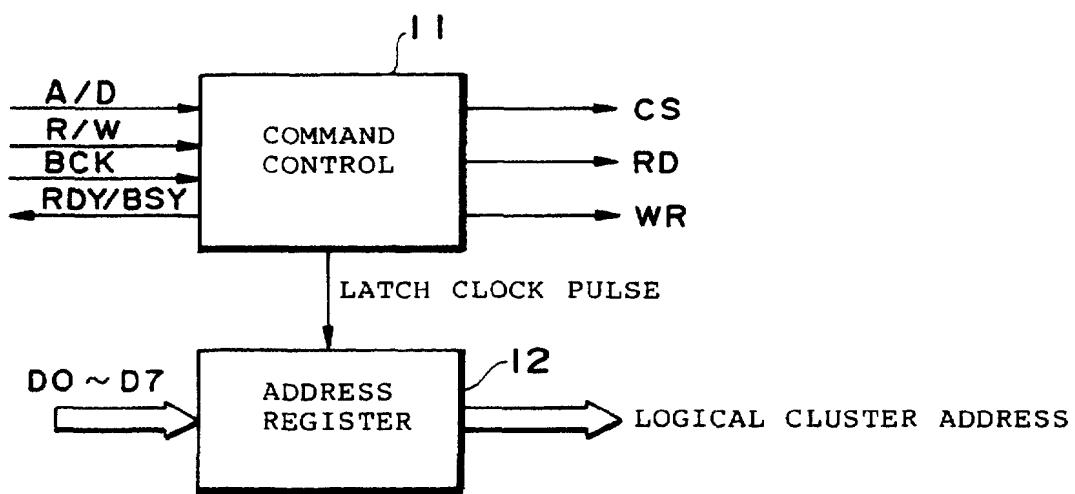
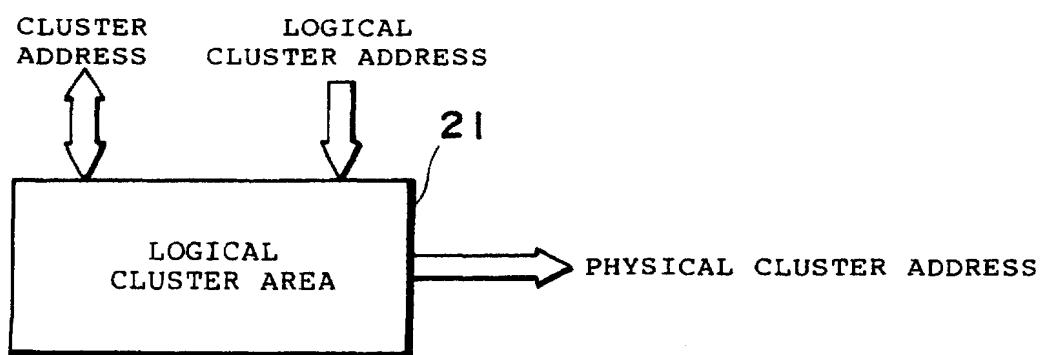
Fig. 2*Fig. 3*

Fig. 4a

LAST-WRITTEN PHYSICAL CLUSTER ADDRESS	LOGICAL CLUSTER ADDRESS	OVER-WRITTEN LOGICAL CLUSTER ADDRESS	LOGICAL CLUSTER AREA
0	0	0	
ad1	0	0	
ad2	0	0	
ad3	0	0	
ad4	0	0	
ad5	0	0	
ad6	0	0	
ad7	0	0	
ad8	0	0	

Fig. 4b

AD1	BLANK STATE	AD2	BLANK STATE	AD3	BLANK STATE	AD4	BLANK STATE	AD5	BLANK STATE	AD6	BLANK STATE	AD7	BLANK STATE	AD8	BLANK STATE	AD9	BLANK STATE	AD10	BLANK STATE	AD11	BLANK STATE	AD12	BLANK STATE
PHYSICAL CLUSTER AREA																							

Fig. 5a

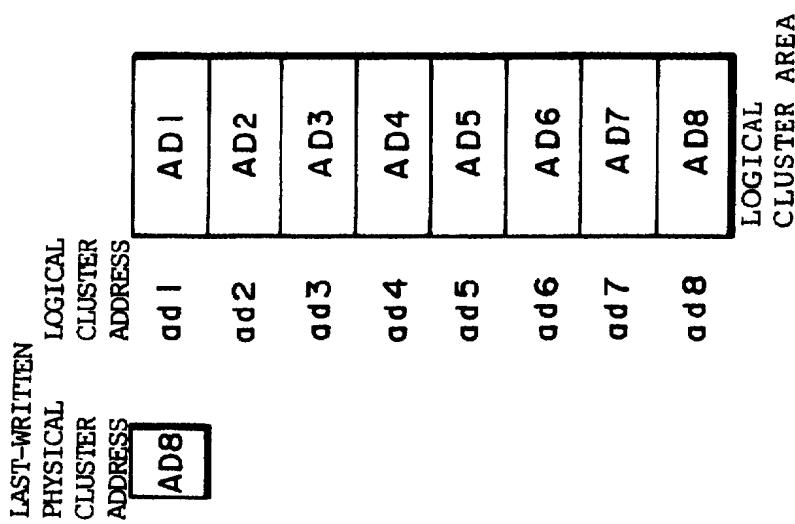


Fig. 5b

LAST-WRITTEN PHYSICAL CLUSTER ADDRESS	LOGICAL CLUSTER ADDRESS	OVER-WRITTEN LOGICAL CLUSTER ADDRESS	LOGICAL CLUSTER AREA	PHYSICAL CLUSTER ADDRESS	CLUSTER DATA	PHYSICAL CLUSTER AREA
ad1	AD1			AD1	CLUSTER DATA CLD1 (A ₁ , B ₁ , C ₁ , D ₁)	
ad2	AD2			AD2	CLUSTER DATA CLD2 (A ₂ , B ₂ , C ₂ , D ₂)	
ad3	AD3			AD3	CLUSTER DATA CLD3 (A ₃ , B ₃ , C ₃ , D ₃)	
ad4	AD4			AD4	CLUSTER DATA CLD4 (A ₄ , B ₄ , C ₄ , D ₄)	
ad5	AD5			AD5	CLUSTER DATA CLD5 (A ₅ , B ₅ , C ₅ , D ₅)	
ad6	AD6			AD6	CLUSTER DATA CLD6 (A ₆ , B ₆ , C ₆ , D ₆)	
ad7	AD7			AD7	CLUSTER DATA CLD7 (A ₇ , B ₇ , C ₇ , D ₇)	
ad8	AD8			AD8	CLUSTER DATA CLD8 (A ₈ , B ₈ , C ₈ , D ₈)	
		0		AD9	BLANK STATE	
				AD10	BLANK STATE	
				AD11	BLANK STATE	
				AD12	BLANK STATE	

Fig. 6a

LAST-WRITTEN PHYSICAL CLUSTER ADDRESS	LOGICAL CLUSTER ADDRESS	OVER-WRITTEN LOGICAL CLUSTER ADDRESS
AD9	AD1	0
ad2	AD9	
ad3	AD3	
ad4	AD4	
ad5	AD5	
ad6	AD6	
ad7	AD7	
ad8	AD8	

LOGICAL
CLUSTER AREA

Fig. 6b

LAST-WRITTEN PHYSICAL CLUSTER ADDRESS	LOGICAL CLUSTER ADDRESS	OVER-WRITTEN LOGICAL CLUSTER ADDRESS	PHYSICAL CLUSTER ADDRESS
AD1			CLUSTER DATA CLD1 (A1, B1, C1, D1)
AD2			DEFECTIVE AREA
AD3			CLUSTER DATA CLD3 (A3, B3, C3, D3)
AD4			CLUSTER DATA CLD4 (A4, B4, C4, D4)
AD5			CLUSTER DATA CLD5 (A5, B5, C5, D5)
AD6			CLUSTER DATA CLD6 (A6, B6, C6, D6)
AD7			CLUSTER DATA CLD7 (A7, B7, C7, D7)
AD8			CLUSTER DATA CLD8 (A8, B8, C8, D8)
AD9			CLUSTER DATA CLD2 (A2, B2, C2, E2)
AD10			BLANK STATE
AD11			BLANK STATE
AD12			BLANK STATE

PHYSICAL CLUSTER AREA

Fig. 7a

LAST-WRITTEN PHYSICAL CLUSTER ADDRESS	LOGICAL CLUSTER ADDRESS	OVER-WRITTEN LOGICAL CLUSTER ADDRESS
AD10	AD1	ad3
ad2	AD9	
ad3	AD10	
ad4	AD4	
ad5	AD5	
ad6	AD6	
ad7	AD7	
ad8	AD8	
		LOGICAL CLUSTER AREA

Fig. 7b

AD1	AD2	AD3	AD4	AD5	AD6	AD7	AD8	AD9	AD10	AD11	AD12	PHYSICAL CLUSTER AREA
CLUSTER DATA CLD1 (A ₁ , B ₁ , C ₁ , D ₁)	DEFECTIVE AREA	BLANK STATE	CLUSTER DATA CLD4 (A ₄ , B ₄ , C ₄ , D ₄)	CLUSTER DATA CLD5 (A ₅ , B ₅ , C ₅ , D ₅)	CLUSTER DATA CLD6 (A ₆ , B ₆ , C ₆ , D ₆)	CLUSTER DATA CLD7 (A ₇ , B ₇ , C ₇ , D ₇)	CLUSTER DATA CLD8 (A ₈ , B ₈ , C ₈ , D ₈)	CLUSTER DATA CLD2 (A ₂ , B ₂ , C ₂ , E ₂)	CLUSTER DATA CLD3 (A ₃ , B ₃ , C ₃ , D ₃)	BLANK STATE	BLANK STATE	

Fig. 8a

LAST-WRITTEN PHYSICAL CLUSTER ADDRESS	LOGICAL CLUSTER ADDRESS	OVER-WRITTEN LOGICAL CLUSTER ADDRESS
AD10	AD1	ad4
ad2	AD9	
ad3	AD10	
ad4	AD3	
ad5	AD5	
ad6	AD6	
ad7	AD7	
ad8	AD8	
		LOGICAL CLUSTER AREA

Fig. 8b

LAST-WRITTEN PHYSICAL CLUSTER ADDRESS	LOGICAL CLUSTER ADDRESS	OVER-WRITTEN LOGICAL CLUSTER ADDRESS	PHYSICAL CLUSTER ADDRESS	LAST-WRITTEN PHYSICAL CLUSTER ADDRESS
AD1			AD1	CLUSTER DATA CLD1 (A ₁ , B ₁ , C ₁ , D ₁)
			AD2	DEFECTIVE AREA
			AD3	CLUSTER DATA CLD4 (A ₄ , B ₄ , C ₄ , D ₄)
			AD4	BLANK STATE
			AD5	CLUSTER DATA CLD5 (A ₅ , B ₅ , C ₅ , D ₅)
			AD6	CLUSTER DATA CLD6 (A ₆ , B ₆ , C ₆ , D ₆)
			AD7	CLUSTER DATA CLD7 (A ₇ , B ₇ , C ₇ , D ₇)
			AD8	CLUSTER DATA CLD8 (A ₈ , B ₈ , C ₈ , D ₈)
			AD9	CLUSTER DATA CLD2 (A ₂ , B ₂ , C ₂ , E ₂)
			AD10	CLUSTER DATA CLD3 (A ₃ , B ₃ , C ₃ , D ₃)
			AD11	BLANK STATE
			AD12	BLANK STATE
				PHYSICAL CLUSTER AREA

Fig. 9a

LAST-WRITTEN PHYSICAL CLUSTER ADDRESS	LOGICAL CLUSTER ADDRESS	OVER-WRITTEN LOGICAL CLUSTER ADDRESS	LOGICAL CLUSTER AREA
AD11	AD1	ad5	
ad2	AD9		
ad3	AD10		
ad4	AD3		
ad5	AD11		
ad6	AD6		
ad7	AD7		
ad8	AD8		

Fig. 9b

LAST-WRITTEN PHYSICAL CLUSTER ADDRESS	LOGICAL CLUSTER ADDRESS	OVER-WRITTEN LOGICAL CLUSTER ADDRESS	LOGICAL CLUSTER AREA	PHYSICAL CLUSTER ADDRESS
AD1	AD1			CLUSTER DATA CLD1 (A ₁ , B ₁ , C ₁ , D ₁)
AD2				DEFECTIVE AREA
AD3				CLUSTER DATA CLD4 (A ₄ , B ₄ , C ₄ , D ₄)
AD4				DEFECTIVE AREA
AD5				BLANK STATE
AD6				CLUSTER DATA CLD6 (A ₆ , B ₆ , C ₆ , D ₆)
AD7				CLUSTER DATA CLD7 (A ₇ , B ₇ , C ₇ , D ₇)
AD8				CLUSTER DATA CLD8 (A ₈ , B ₈ , C ₈ , D ₈)
AD9				CLUSTER DATA CLD2 (A ₂ , B ₂ , C ₂ , E ₂)
AD10				CLUSTER DATA CLD3 (A ₃ , B ₃ , C ₃ , D ₃)
AD11				CLUSTER DATA CLD5 (A ₅ , B ₅ , C ₅ , E ₅)
AD12				BLANK STATE
				PHYSICAL CLUSTER AREA



Europäisches Patentamt
European Patent Office
Office européen des brevets



(11) Publication number:

0 557 968 A3

(12)

EUROPEAN PATENT APPLICATION

(21) Application number: 93102875.7

(51) Int. Cl.⁵: **G11C 16/06, G11C 11/00**

(22) Date of filing: **24.02.93**

(30) Priority: **25.02.92 JP 73255/92**

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(43) Date of publication of application:
01.09.93 Bulletin 93/35

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(84) Designated Contracting States:
DE FR GB

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(86) Date of deferred publication of the search report:
30.03.94 Bulletin 94/13

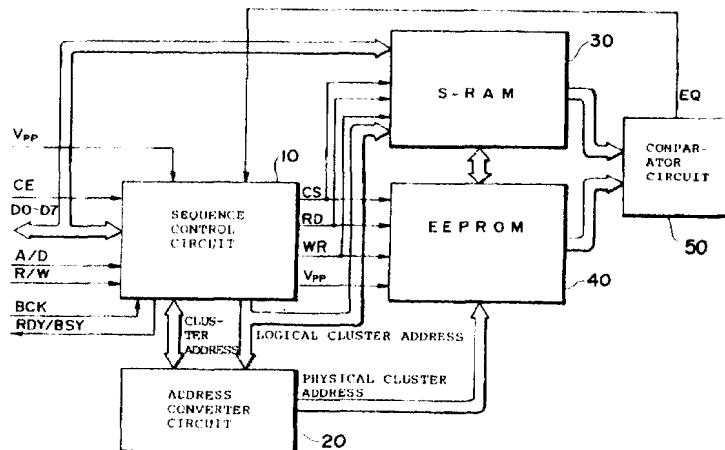
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(54) Method of rewriting data in EEPROM, and EEPROM card.

(57) A memory card includes an S-RAM in addition to an EEPROM. When old data constituting part of data that has been recorded in the EEPROM is to be rewritten, the old data to be rewritten is read out of the EEPROM and applied to the S-RAM, where the old data is temporarily stored. The old data in the S-RAM is rewritten to new data, and the new data is applied to and written in the EEPROM. A comparator

circuit determines whether all bits of the new data rewritten in the S-RAM and all bits of the new data written in the EEPROM coincide. If all bits coincide, this is verification that the changed data has been stored in the EEPROM correctly. Thus, the reliability with which data is rewritten in the EEPROM is improved.

Fig. 1



EP 0 557 968 A3



European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 93 10 2875

DOCUMENTS CONSIDERED TO BE RELEVANT			CLASSIFICATION OF THE APPLICATION (Int.CI.S)
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	
E	EP-A-0 528 280 (KABUSHIKI KAISHA TOSHIBA) * column 7, line 10 - column 11, line 28; figures 2,3 * * column 18, line 37 - column 20, line 57; figures 10,11 * * column 24, line 1 - line 45; figure 16 * ---	1-9	G11C16/06 G11C11/00
A	PATENT ABSTRACTS OF JAPAN vol. 8, no. 179 (P-295)(1616) 17 August 1984 & JP-A-59 071 180 (DAINIPPON INSATSU KK) 21 April 1984 * abstract * ---	1,2,7	
A	US-A-4 402 065 (TAYLOR) * the whole document * -----	1,7	
The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int.CI.S)
			G11C G06F
<p>Place of search</p> <p>THE HAGUE</p> <p>Category of cited documents</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons A : member of the same patent family, corresponding document</p>			
<p>Date of completion of the search</p> <p>28 January 1994</p>			Examiner Cummings, A